Disruptive Developments for Advanced Die Attach to Tackle the Challenges of Heterogeneous Integration

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ECTC 2018 / San Diego

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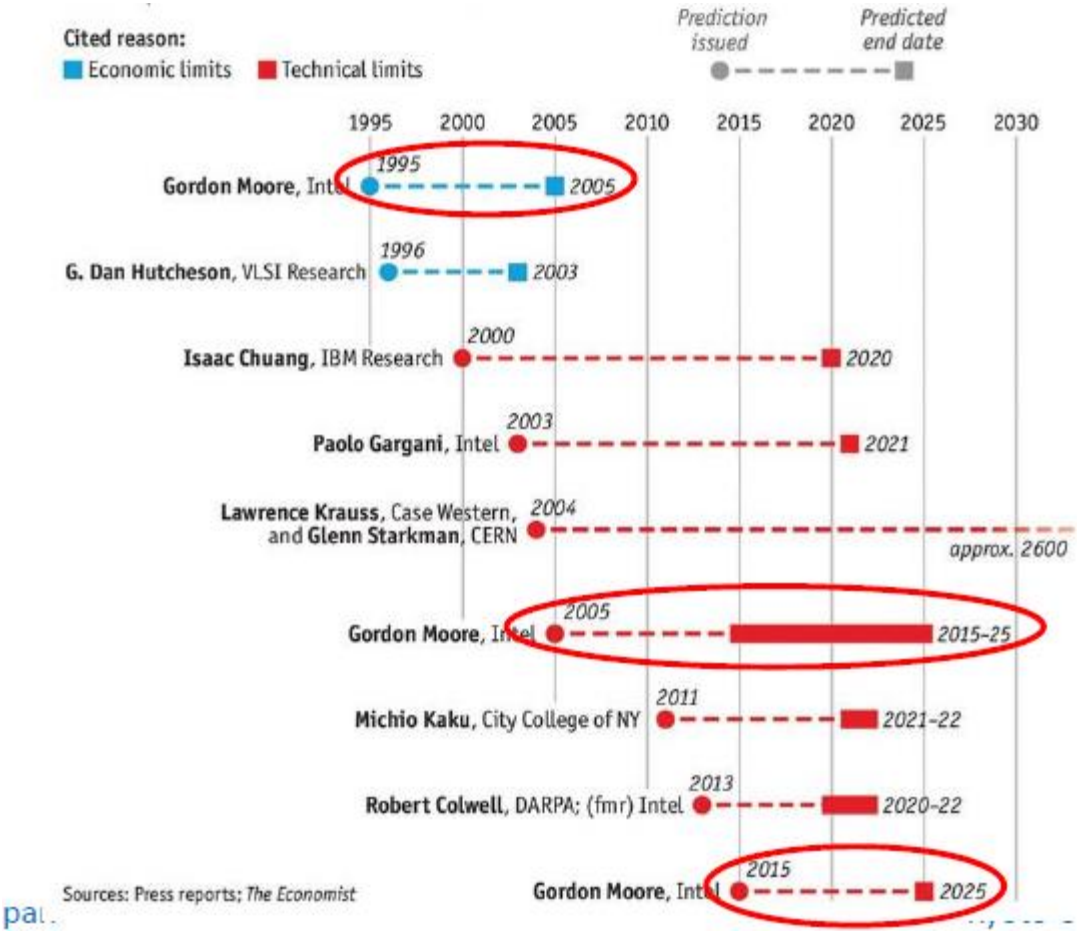
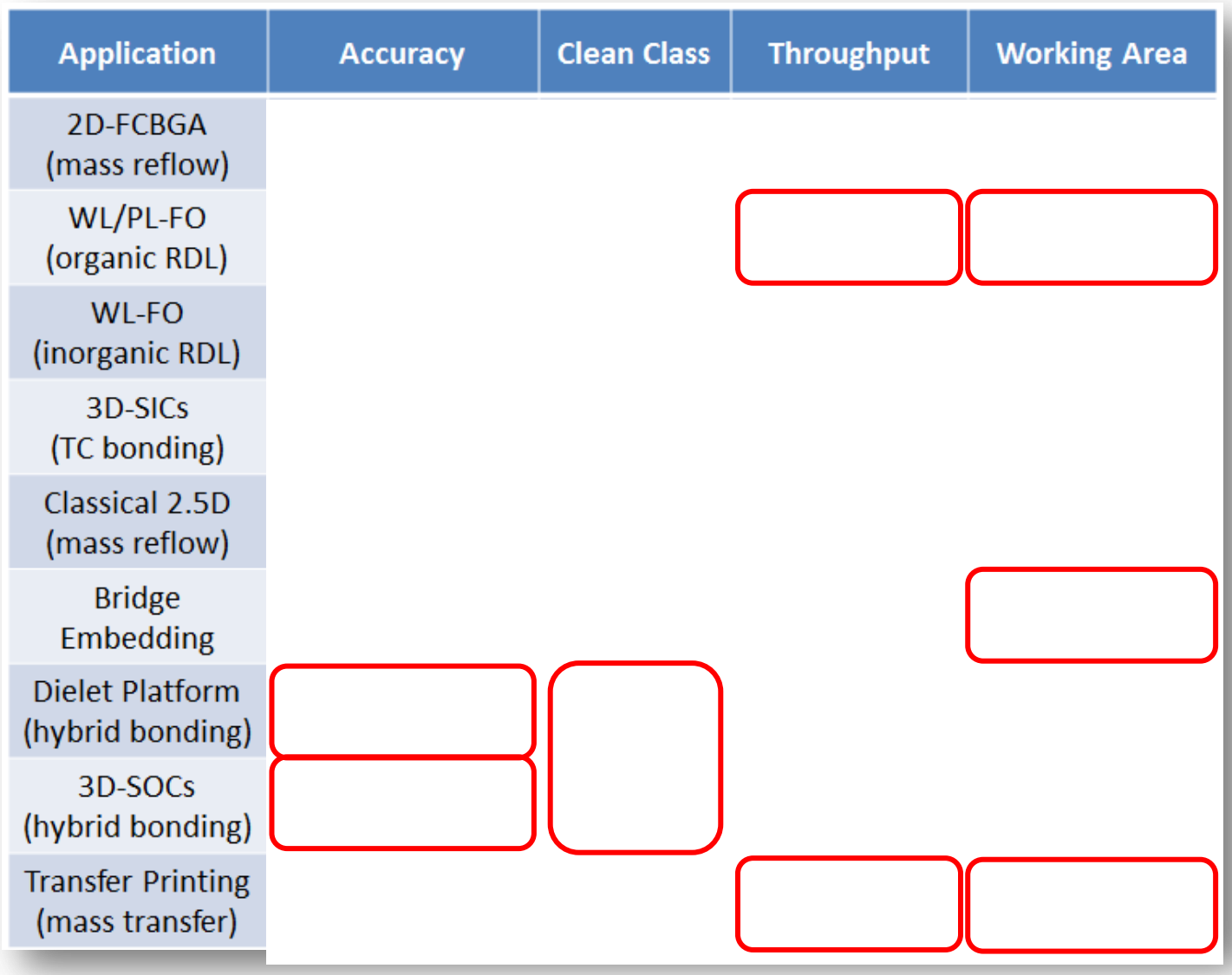
- Introduction
- Current Integration Architectures
- Future Integration Architectures
- Demand for High Capabilities
- Disruptive Developments
- Conclusions & Take-aways

Is the End of Moore's Law Coming?



Many predictions of the end of Moore's Law
(last prediction by Gordon Moore -> 2025)

Enhanced Capabilities Demanded



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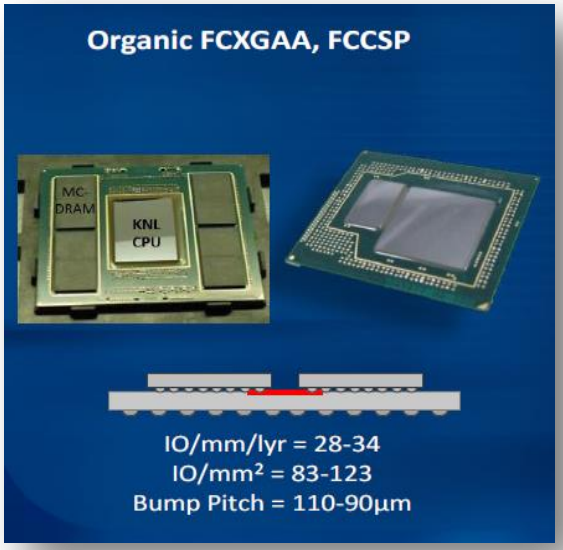
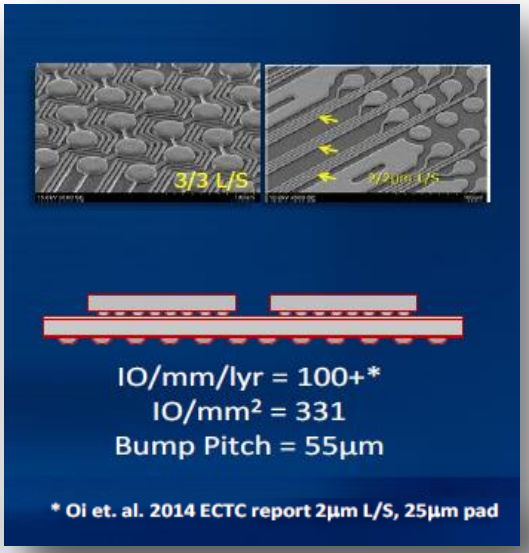
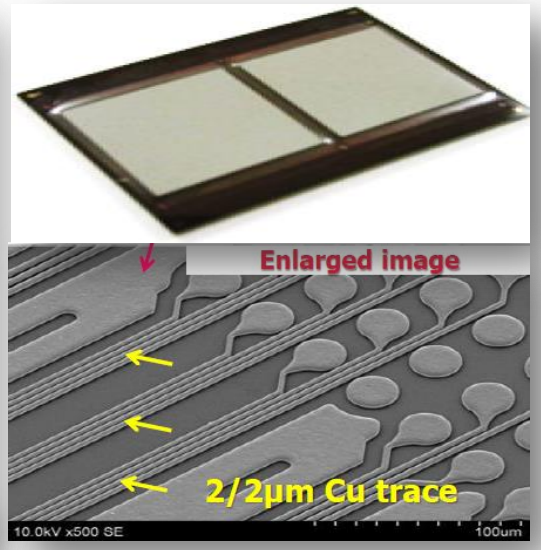
2D-Side-by-Side Packages





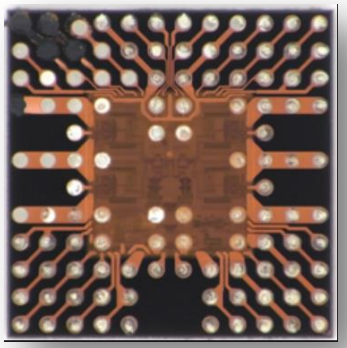
Intel's Knights Landing™



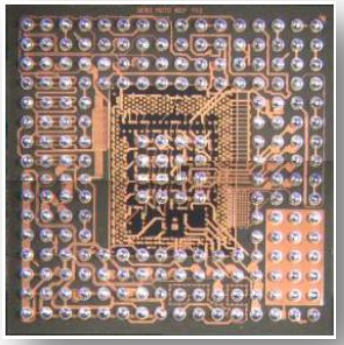
Shinko's i-THOP™ laminate

- Conventional 2D Multi Chip Package architectures, typically FC-BGA,
- Either MR-FC bonding or TC-Bonding
- Interconnection of active side-by-side die is accomplished by either (wire bonded) wires and/or substrate traces

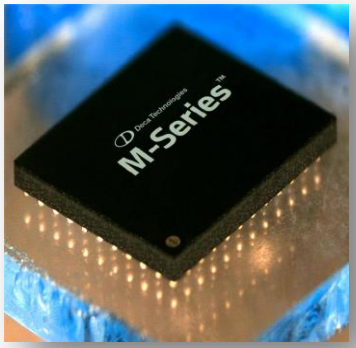
Organic RDL Based Packages



Infineon's eWLB

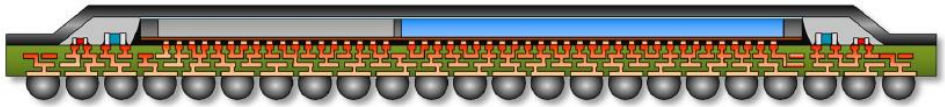


Freescale's RCP



Deca's M-series

Amkor's SWIFT

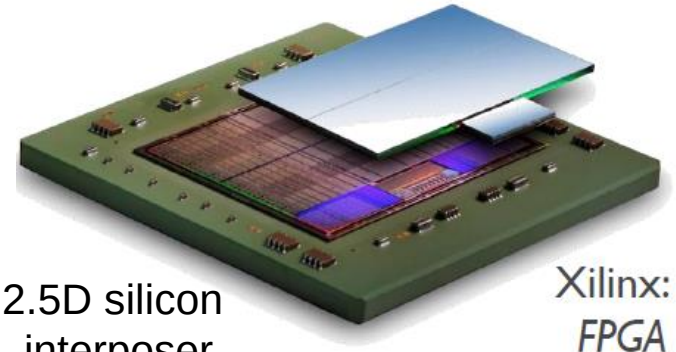


ASE's FOCoS

TSMC InFO

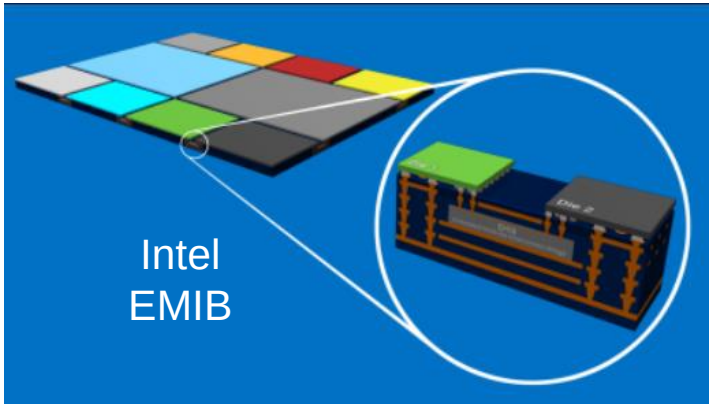
- Organic RDL based WL/PL-Fan-out packaging technology
- Interconnection of active side-by-side die is accomplished by an organic redistribution layer (RDL)

Inorganic RDL Based Packages



2.5D silicon interposer package

Xilinx:
FPGA
Virtex-7 H580T

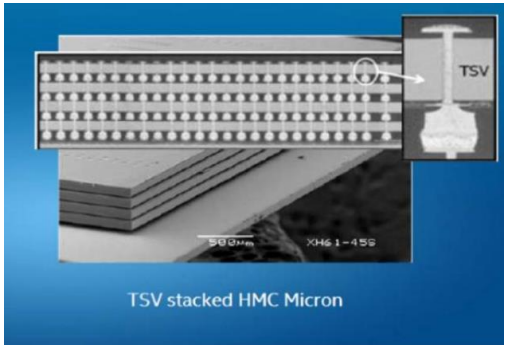


CoWoS

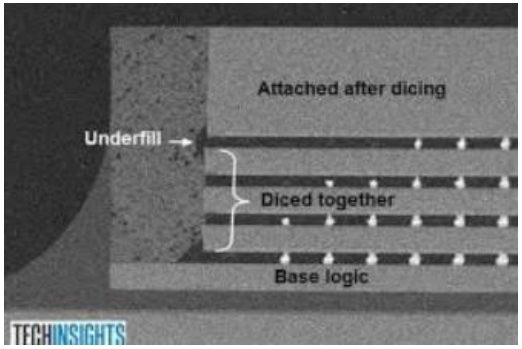
Based on inorganic RDL (silicon oxide, silicon nitride)

- a) 2.5D TSV based or TSV-less silicon or glass interposer packaging
- b) embedded silicon bridges (EMIB™)
- c) CoWoS (Chip on wafer on Substrate): 2.5D Si-interposer on substrate

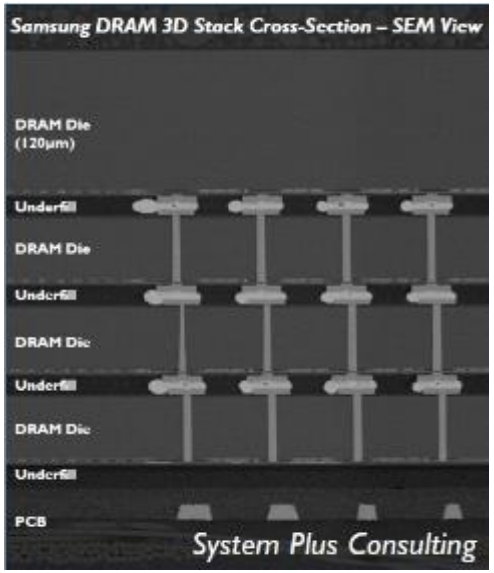
3D-Stacked IC (3D-SIC)



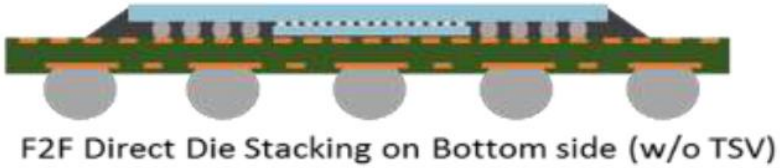
Hybrid Memory Cube
(HMC)



High Bandwidth Memory
(HBM)



Stacked DRAM
(3DS)



Amkor's Possum™
(F2F)

- Direct interconnected active die which are 3D arranged
- a) 3D TSV based packaging
- b) 3D Face-to-face packaging

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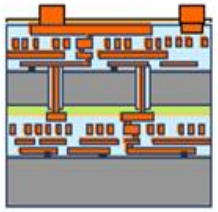
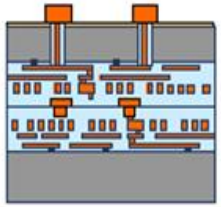
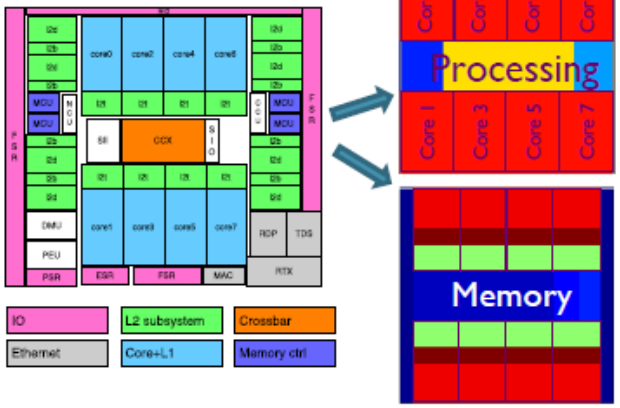
3D-SOCs

	3D-SIC	3D-SOC		
wiring level	Global	Semi-global	Intermediate	Local
2-tier stack				
Contact Pitch *Relative density:*	40 ⇒20 ⇒10 ⇒*5µm* 1/16⇒¼ ⇒1 ⇒ 4	5 ⇒ 1 µm 4 ⇒ 100	2 µm ⇒ 0.5 µm 50 ⇒ 400	200 ⇒ 100 nm 5000 ⇒ 10000
Partitioning	Die	**blocks** of standard cells		**Gates**

IMEC
3D-Roadmap

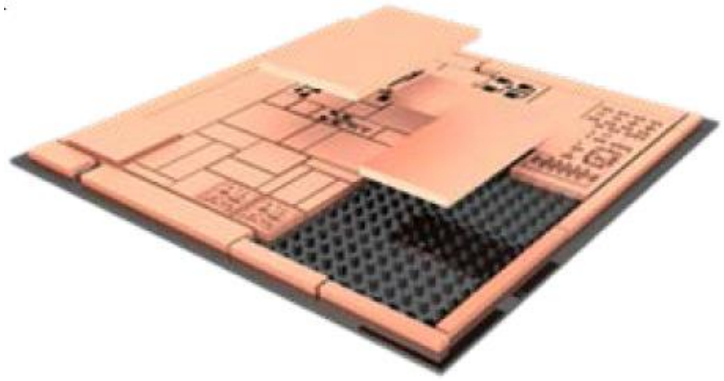
OpenSPARC T2

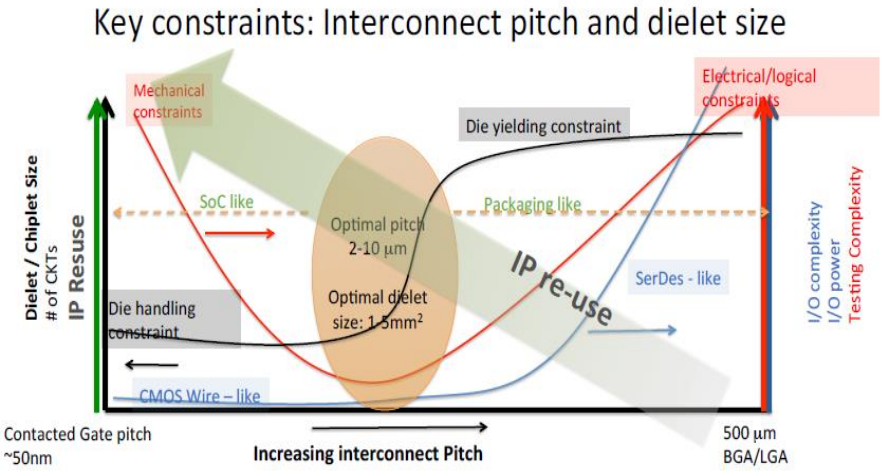


3D-SOC Study for
OpenSPARC T2
to be 3D-integrated
into
Logic + Memory

Source: Philipp Absil, "Overview of the 3D Technology Landscape And Challenges", Semicon korea 2016:

2.5D Chiplet (Dielet) Platforms





DARPA's CHIPS Program [1]

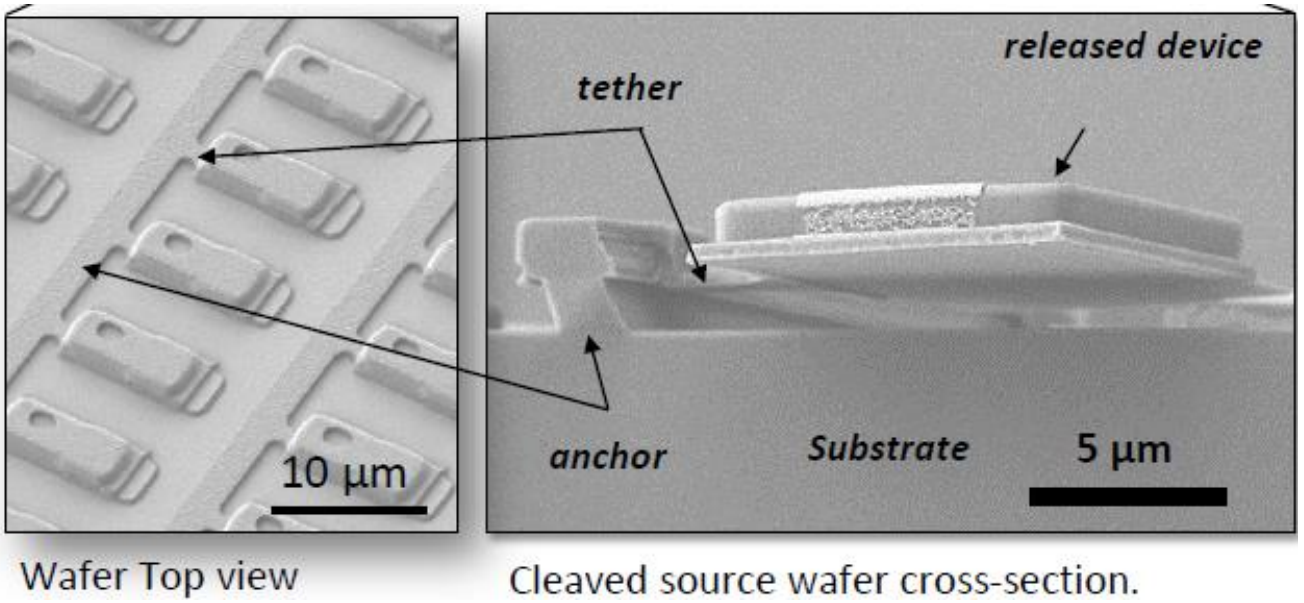
- CHIPS = chiplet (dielet) platform
- Chiplet = functional, verified, re-usable IP block, realized in physical form [2]

Pitch sweet spot between 2 and 10µm for chiplet (dielet) based HI platforms [3]

Source:
[1] D.S. Green, "DARPA's CHIPS Program, and Making Heterogeneous Integration Common", 3D-ASIP 2017
[2] S. Shumarayev, "Heterogeneous Platform – Innovation with Partners", 3D ASIP 2017
[3] S. Iyer, "3D-SOCs Through Advanced Packaging", 3D-ASIP 2016

Transfer Printing

- Example of transfer-print compatible micro devices
- Devices are undercut and anchored using MEMS-processing technologies
- Throughput proposals beyond 300.000 components/hour
- 1.5µ @ 3σ accuracy required



Source: Kanchan Ghosal / X-Celeprint:
"Mass Transfer of Microscale Devices Using Transfer Printing, 3D ASIP Conference, 2017

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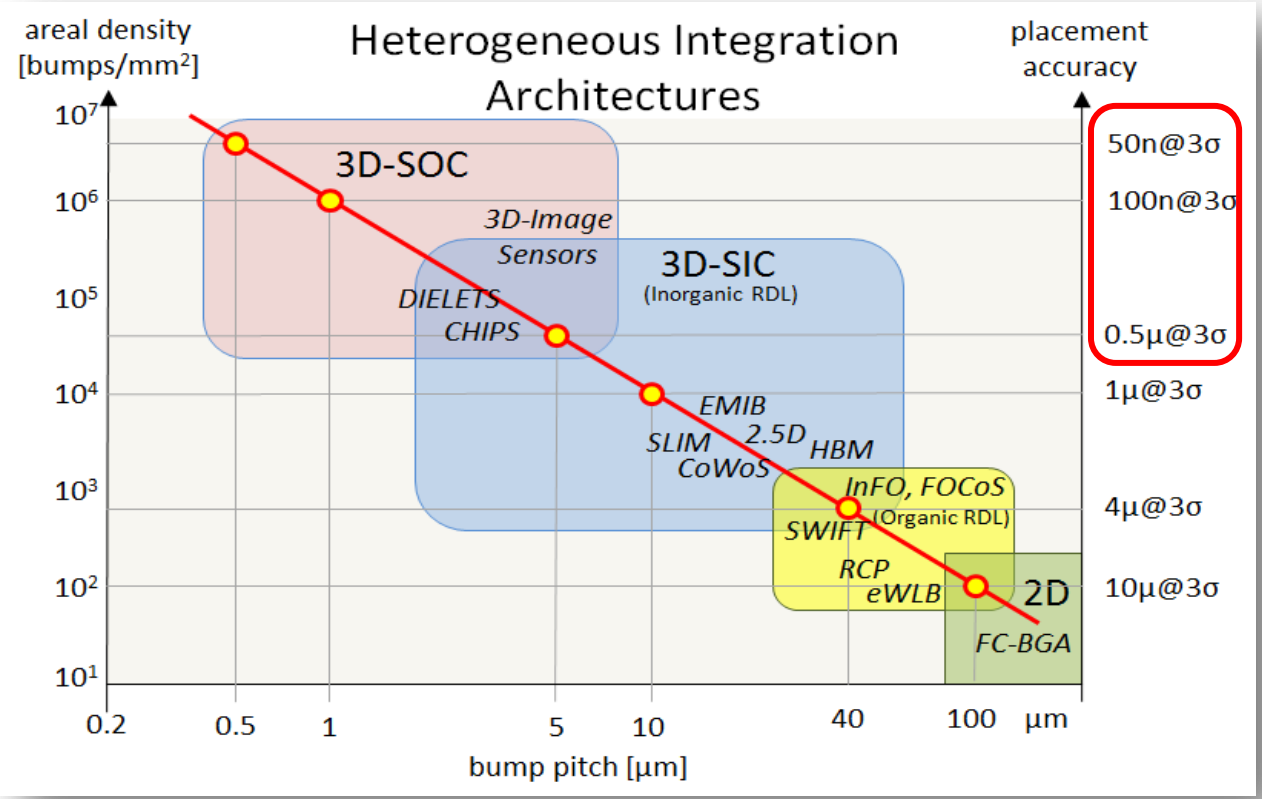
Drive for Higher Accuracy



comparison of Heterogeneous Integration architectures according to bump pitch metrics and areal density

areal density = 1 / (bump pitch)^2

placement accuracy @ 3σ ≈ (bump pitch) / 10 *)

*) center accuracy for self centering processes, like MR-FC
corner accuracy for non self centering (FO, TC, hybrid bonding)

Enhanced Capabilities Demanded

present

future

Application	Accuracy	Clean Class	Throughput	Working Area
2D-FCBGA (mass reflow)	5-10µ@3σ (die center)	ISO-6	15-20 kCPH	300 x 125 mm
WL/PL-FO (organic RDL)	3-10µ@3σ (die corners)	ISO-5	15-40 kCPH	ϕ 300 mm 650 x 550 mm
WL-FO a) (inorganic RDL)	2-3µ@3σ (die corners)	ISO-5	5-10 kCPH	ϕ 300 mm
3D-SICs (TC bonding)	2-3µ@3σ (die corners)	ISO-5	3-5 kCPH (tack & gang)	ϕ 300 mm
Classical 2.5D c) (mass reflow)	3-5µ@3σ (die center)	ISO-5	5-10 kCPH	ϕ 300 mm
Bridge b) Embedding	0.5-2µ@3σ (die corners)	ISO-4	2-5 kCPH	650 x 550 mm
Dielet Platform (hybrid bonding)	0.2-1µ@3σ (die corners)	ISO-3 (ISO-2)	5-10 kCPH	ϕ 300 mm
3D-SOCs (hybrid bonding)	50-500nm@3σ (die corners)	ISO-3 (ISO-2)	1-5 kCPH	ϕ 300 mm
Transfer Printing (mass transfer)	0.5-2µ@3σ (die corners)	ISO-5 (ISO-4)	50–300 kCPH	650 x 550 mm (920 x 730 mm)

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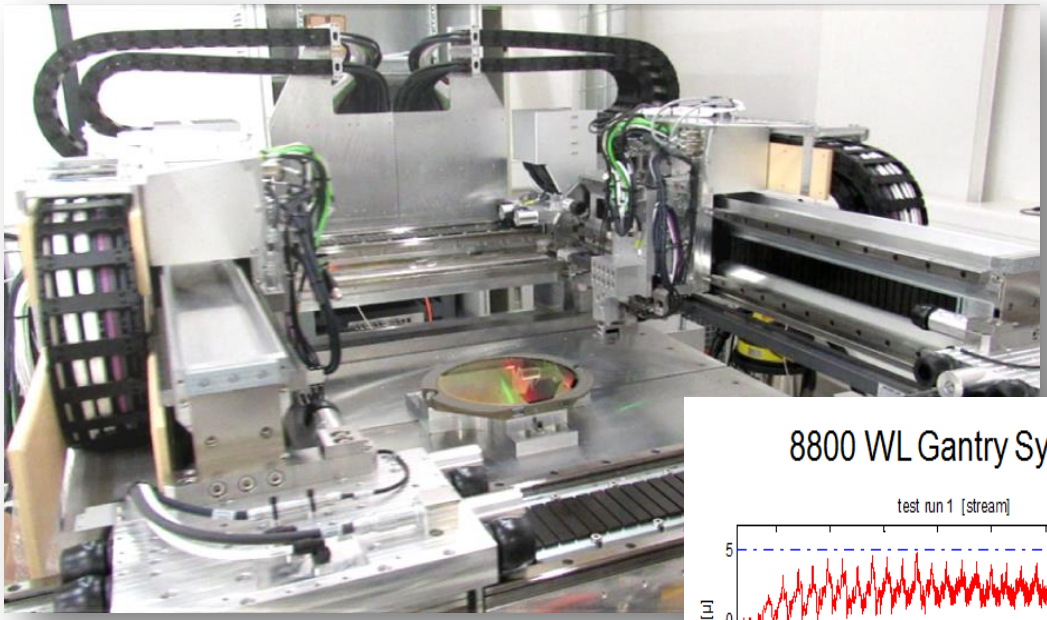
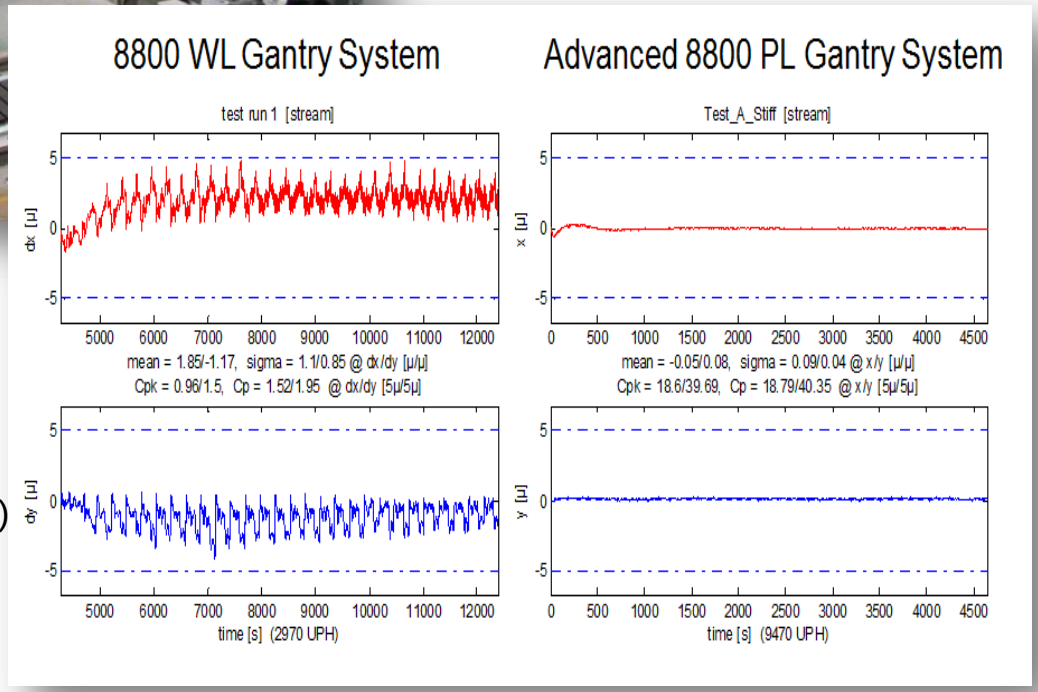
Advanced Gantry System



Advanced Gantry System

- Decoupled metrology
- Water cooled



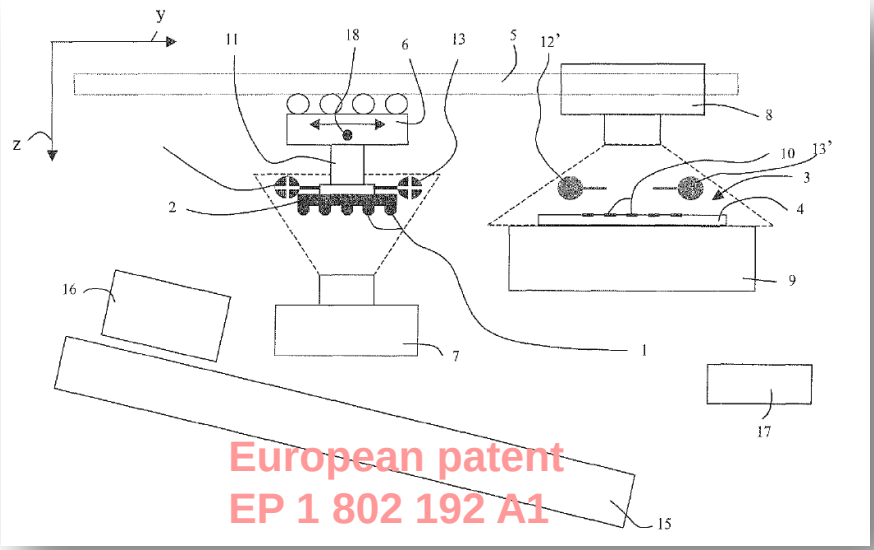
Strength

- 2µ@3σ global*)
  pick & place accuracy
- Roadmap: 1µ@3σ global*)
  pick & place accuracy

*) ‘global‘ means: no local fiducials!

‘Van Gogh Alignment’ Method

To achieve 200nm@3σ placement accuracy (@ 1000 UPH)

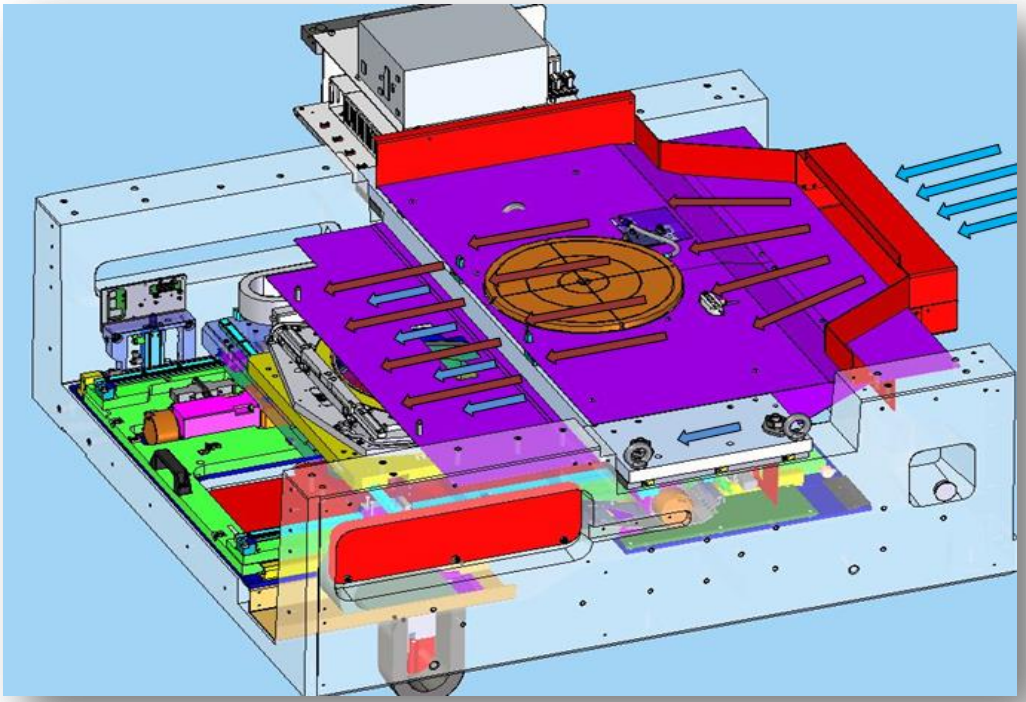


Principle

1. tool reference marks next to the die
2. upward camera determines position of die fiducial relative to tool reference mark
3. downward camera determines position of substrate fiducial relative to tool reference mark
4. Calculation of resulting misalignment and correction with ‚Nano Actor‘

Enhanced Clean Capability

ISO-3 clean concept for Datacon 8800 platform

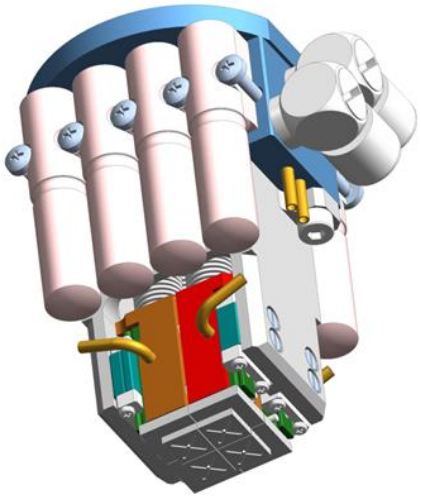


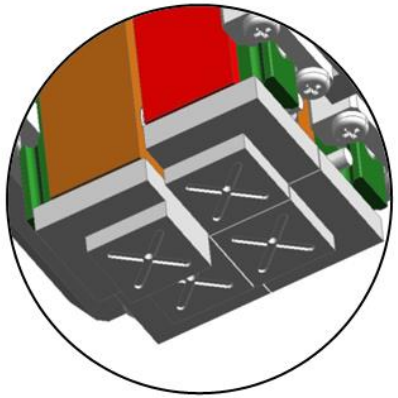
1. Use of ISO-3 compatible cables & vacuum hoses
2. Covering all energy chains – exhaust dirty air from inside of covers
3. Introducing horizonal, HEPA filter cleaned laminar flow
4. Loading substrate and diced wafers from FOUPs via EFEMs

Parallel Die Processing

Multi-nozzle bond head concept for Datacon 8800 platform

- Common z-axis for 4 nozzles
- Individual mini-stroke per nozzle to move nozzle into working or standby position





Throughput Target:

- 20.000+ chips/hour
- ϕ300 or 650x550 mm

1. Sequential picking of dies
2. Concurrent (parallel) transfer of 4 dies
3. Concurrent (parallel) upward vision of 4 dies
4. Sequential bonding of dies

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Conclusions & Take Aways

- Advanced Die Attach will be in future a key technology for Heterogeneous Integration.
- Roadmaps are proposing 40->10µ pitch for 2.5D/3D SIC, 10-2µ pitch for dielet/chiplet 2.5D platforms, and 5->1µ pitch for 3D-SOCs.
- Hybrid bonding is believed to be the killer technology for sub micron W2W, D2D or D2W 2.5D/3D integration architectures
- hybrid bonding is driving sub-µm placement accuracy with ultra clean conditions (ISO3->ISO2), while cost down drives throughput beyond 20.000 UPH on GEN-3 panel level (650 x 550 mm)
- 4 disruptive developments for Advanced Die Attach
  - Water cooled Advanced Gantry System based on decoupled metrology
  - ‘Van Gogh Alignment’ method for nanometer scale placement accuracy
  - ISO-3 clean concept for 8800 advanced die attach platform
  - Quattro-nozzle bond head for parallel die transfer and sequential pick/place

Thank You!